Solution to Homework 5

Nov. 25, 2014

Prob 1.

Signal flow of Problem 1.

Block diagram of overall architecture.

1 register : +5, 2 registers : +10
Z Iteration checker (with Up or Down Counter) : +10

4-bit adder computing X+Y : 10

When the sum exceeds 15, it wraps around 0 : +2

'Start' signal interconnection to registers : =2
Clock interconnection : +2
Current output is Y : +2
By inspection (or can use K-maps):

\[ Q^+ = Q \oplus x \]

\[ Z_1 = Q \oplus x = Q^+ \]

\[ Z_2 = Q' \oplus x \]

Alternatively, \( Z_2 = \overline{Z_1} \), so it's possible to replace the second XOR with a NOT on the output (or any other logic that works).
Additionally, I + J will never be reached for a non-initialized machine. 5 pt

Same goes for G/H, but it outputs to itself so it can occur in a non initial cycle if it was the initial state.